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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
TSE, YOUNG TOI	
ART UNIT	**PAPER NUMBER**
2634	12

DATE MAILED: 04/05/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/644,532	HE, RUNSHENG	
	Examiner	Art Unit	
	YOUNG T. TSE	2634	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 December 2003*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-74* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8,10-28,30-45,47-65 and 67-74* is/are rejected.

7)☒ Claim(s) *9,29,46 and 66* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *24 August 2000* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Drawings

1. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they include the following reference sign(s) not mentioned in the description: the reference signs 112 of Figure 1 and 312 of Figure 3 are not mentioned in the specification. A proposed drawing correction, corrected drawings, or amendment to the specification to add the reference sign(s) in the description, are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

2. The drawings were received on 30 December 2003. These drawings are acceptable.

Claim Objections

3. Claims 7-9, 13, 15-17, 27-29, 33, 35-38, 44-46, 50, 52, 64, -66, 70, and 73-74 are objected to because of the following informalities: in claim 7, lines 6-7, "a first finite impulse response filter (FIR)" should be -- a finite impulse response (FIR) filter --; in claim 8, line 2, "said first FIR filter" should be -- said FIR filter --; in claim 9, lines 6-7, "a first finite impulse response filter (FIR)" should be -- a first finite impulse response (FIR) filter --; in claim 13, line 2, "a first adaptive control circuit" should be -- an adaptive control circuit --; in claim 15, line 2, "said first adaptive control circuit" should be -- said adaptive control circuit --; in claim 16, line 2, "a second finite impulse response filter

(FIR)" should be -- a finite impulse response (FIR) filter --; in claim 17, line 2, "a second adaptive control circuit" and "said second FIR" should be -- an adaptive control circuit -- and -- said FIR filter --, respectively; in claim 27, lines 6-7, "a first finite impulse response filter (FIR) means" should be -- a finite impulse response (FIR) filter means --; in claim 28, line 2, "said first FIR filter means" should be -- said FIR filter means --; in claim 29, lines 6-7, 8 and 10, "a first finite impulse response filter (FIR) means" and "said first FIR filter means" should be -- a finite impulse response (FIR) filter means -- and -- said FIR filter means --; in claim 33, line 2, "a first adaptive control means" should be -- an adaptive control means --; in claim 35, line 2, "said first adaptive control means" should be -- said adaptive control means --; in claim 36, lines 2-3, "a second finite impulse response filter (FIR) means" should be -- a finite impulse response (FIR) filter means --; in claim 37, lines 2-3, "a second adaptive control means" and "said second FIR means" should be -- an adaptive control means -- and -- said FIR filter means --, respectively; in claim 38, line 3, "an output" should be -- an output circuit --; in claim 44, lines 4 and 8-9, "an output" and "a first finite impulse response filter (FIR)" should be -- an output circuit -- and -- a first finite impulse response (FIR) filter --, respectively; in claim 45, lines 1-2, "said first FIR filter" should be -- said FIR filter --; in claim 46, lines 4, 8, 10, and 12, "an output", "a first finite impulse response filter (FIR)", and "said first FIR filter" should be -- an output circuit --, -- a finite impulse response (FIR) filter --, and -- said FIR filter --; in claim 50, line 2, "a first adaptive control circuit" should be -- an adaptive control circuit --; in claim 52, lines 1-2, "said first adaptive control circuit" should be -- said adaptive control circuit --; in claim 64, lines 6-7, "a first finite impulse response

filter (FIR) means" should be -- a finite impulse response (FIR) filter means --; in claim 65, lines 1-2, "said first FIR filter means" should be -- said FIR filter means --; in claim 66, lines 6-7, 8 and 10, "a first finite impulse response filter (FIR) means" and "said first FIR filter means" should be -- a finite impulse response (FIR) filter means – and -- said FIR filter means --; in claim 70, line 2, "a first adaptive control means" should be -- an adaptive control means --; in claim 73, line 2, "a second finite impulse response filter (FIR) means" should be -- a finite impulse response (FIR) filter means --; and in claim 74, line 2, "a second adaptive control means" and "said second FIR means should be -- an adaptive control means – and – said FIR filter means --, respectively. Appropriate correction is required.

Claim Rejections - 35 USC § 112

4. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

5. Claims 19-25, 57-62, and 71 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In line 1 of claims 19-25 and lines 1-2 of claims 57-62, the phrase "said feedforward equalizer" lacks clear antecedent basis.

Claim 71 recites an Ethernet transceiver according to claim 33, however, claim 33 recites a signal processing apparatus. Further, Applicant is requested to clarify the difference between claim 71 and claim 34.

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

7. Claims 1-8, 1-12, 16-28, 30-33, 35-45, 47-50, 52-65, 67-70, and 72-74 are rejected under 35 U.S.C. 102(b) as being anticipated by Sayar (Newly cited).

Sayar (US Re. No. 34,206) discloses a U-interface transceiver in Figure 1 comprising a transmitter and a receiver.

The receiver comprises a channel interface 116, a sigma-delta modulator 118 oversamples the received signal effectively performing an analog-to-digital conversion of the signal (col. 4, lines 60-66), a decimator 120, a high pass receiver filter 126 which serves as a feedforward equalizer and enhances high frequencies (col. 5, lines 15-18), an echo canceller 128, a decision feedback equalizer 130, subtractors 132 and 134, an adaptive threshold slicer 136, and a subtractor 160 (col. 5, lines 58-63).

With respect to claims 1, 7, 18, 27, 38, 44, 55, and 64, the high pass receiver filter 126 is a feedforward equalizer which corresponds to the feedforward filter or high pass filter; the feedback equalizer 130, the subtractors 132 and 134, the adaptive threshold slicer 136, and the subtractor 160 are integrated as a decision feedback equalizer which comprises a decision circuit (132, 134, 136, and 160) and a feedback filter 130.

With respect to claims 7, 16, 27, 36, 44, 53, 64, and 73, it is well known in the art that a decision feedforward or feedback equalizer or filter is a finite impulse response (FIR) filter.

With respect to claims 2-6, 19-22, 24-26, 39-43, and 56-63, it is well known to a person skill in the equalization art that a feedforward or high pass filter has the capability of low cutoff frequency, flat response, high attenuation at low frequency or frequencies, wherein the high attenuation is at least 20 db, DC noise attenuation, and baseline wander.

With respect to claims 8, 13, 15, 17, 28, 33, 35, 37, 45, 50, 52, 54, 65, 70, 72, and 74, the FIR filter of the feedforward or feedback equalizer comprises filter precursor, main taps, and filter postcursor controlled by an adaptive control circuit during signal acquisition is well known in the decision feedback equalizer art, which is also shown in the prior art Figures 1 and 2 of the instant application.

With respect to claims 10-11, 30-31, 47-48, and 67-68, the conversion of converting an analog signal into a digital signal is performed by the sigma-delta modulator 118 and the decision circuit comprises the adaptive threshold slicer 136.

With respect to claims 12, 32, 49, and 69, the decision circuit comprises a Viterbi detector is well known to a person skill in the decision feedback equalizer because a lot of decision feedback equalizers are operated by Viterbi detector or equalizers.

8. Claims 1-8, 1-12, 16-28, 30-33, 35-45, 47-50, 52-65, 67-70, and 72-74 are rejected under 35 U.S.C. 102(b) as being anticipated by Fertner (Newly cited).

Fertner (US Patent No. 5,793,801) discloses a digital communications system in Figure 3 comprising a transmitter and a receiver.

The receiver comprises an A/D converter 48, a receive filter 50, a subtractor 52, an adaptive gain controller 54, a decision feedback equalizer, a decoder 62, a descrambler 64, and a timing recovery 70.

The decision feedback equalizer comprises a feedforward filter 56, a subtractor 58, a detector 60, a subtractor 66, and a decision feedback equalizer 68. Fertner teaches the feedforward filter 56 which in physical terms enhances high frequencies (operated as high pass filter) of pulses in the received signal which translates into an increase in the steepeness or slope of the rising edge of the digital pulse (col. 7, lines 57-62).

With respect to claims 1, 7, 18, 27, 38, 44, 55, and 64, the decision feedforward filter 56 is a high pass receiver filter corresponds to the feedforward filter or high pass filter; the subtractor 58, the detector 60, the subtractor 66, and the decision feedback equalizer 68 are integrated as a decision feedback equalizer which comprises a decision circuit 60 and a decision feedback equalizer or filter 68.

With respect to claims 7, 16, 27, 36, 44, 53, 64, and 73, it is well known in the art that a decision feedforward or feedback equalizer or filter is a finite impulse response (FIR) filter.

With respect to claims 2-6, 19-22, 24-26, 39-43, and 56-63, it is well known to a person skill in the equalization art that a feedforward or high pass filter has the capability of low cutoff frequency, flat response, high attenuation at low frequency or

frequencies, wherein the high attenuation is at least 20 db, DC noise attenuation, and baseline wander.

With respect to claims 8, 13, 15, 17, 28, 33, 35, 37, 45, 50, 52, 54, 65, 70, 72, and 74, the FIR filter of the feedforward or feedback equalizer comprises filter precursor, main taps, and filter postcursor controlled by an adaptive control circuit during signal acquisition is well known in the decision feedback equalizer art, which is also shown in the prior art Figures 1 and 2 of the instant application.

With respect to claims 10-11, 30-31, 47-48, and 67-68, the conversion of converting an analog signal into a digital signal is performed by the A/D converter 48 and the decision circuit comprises a threshold circuit such as the detector 60.

With respect to claims 12, 32, 49, and 69, the decision circuit comprises a Viterbi detector is well known to a person skill in the decision feedback equalizer because a lot of decision feedback equalizers are operated by Viterbi detector or equalizers.

Claim Rejections - 35 USC § 103

9. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

10. Claims 14, 23, 34, 51, and 71 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sayar in view of Samueli et al. (Previously cited).

Although Sayar does not explicitly show or suggest that the feedforward equalizer shortents a length of posrcursor inter-symbol interference as recited in claim 23 and a limiter circuit for limiting the range of adaptation of the postcursors as recited in claims 14, 34, 51, and 71.

Samueli et al. (US patent No. 6,178,198) discloses a decision feedback equalizer in Fig. 5 wherein the feedforward equalizer 102 and the tail canceller 110 are used to reduce the number of taps of the postcursors (col. 9, lines 40-45), further, Samueli also teaches that the high pass filter 100 and the tail canceller 110 inhibit the postcursor response of the digital signals by limiting the time duration of the post cursor response (col. 2, lines 41-44).

Therefore, it would have been obvious to one of ordinary skill in the art to includes a limiter circuit internal or external to Sayar's decision feedback equalizer in order to reduce the number or posrcursor intersymbol interference and have better control of the postcursors of the decision feedback equalizer.

11. Claims 14, 23, 34, 51, and 71 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fertner in view of Samueli et al. (Previously cited).

Although Fertner does not explicitly show or suggest that the feedforward equalizer shortents a length of posrcursor inter-symbol interference as recited in claim 23 and a limiter circuit for limiting the range of adaptation of the postcursors as recited in claims 14, 34, 51, and 71.

Samueli et al. (US patent No. 6,178,198) discloses a decision feedback equalizer in Fig. 5 wherein the feedforward equalizer 102 and the tail canceller 110 are used to

reduce the number of taps of the postcursors (col. 9, lines 40-45), further, Samueli also teaches that the high pass filter 100 and the tail canceller 110 inhibit the postcursor response of the digital signals by limiting the time duration of the post cursor response (col. 2, lines 41-44).

Therefore, it would have been obvious to one of ordinary skill in the art to includes a limiter circuit internal or external to Fertner's decision feedback equalizer in order to reduce the number or posrcursor intersymbol interference and have better control of the postcursors of the decision feedback equalizer.

Allowable Subject Matter

12. Claims 9, 29, 46, and 66 would be allowable if rewritten or amended to overcome the objection(s) set forth in this Office action.

13. The following is a statement of reasons for the indication of allowable subject matter: the prior art fails to show or suggest that summation of the precursors, the main tap (is unity), and the postcursors is greater than 0 (zero) but less than 1 (one). Wherein the main tap is unity and the value of each of the postcursors is greater than –1 but less than 0.

Conclusion

14. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP

§ 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to **Young Tse** whose telephone number is **(703) 305-4736**.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, **Stephen Chin**, can be reached at **(703) 305-4714**.

Any response to this action should be mailed to:

Commissioner of Patents and Trademarks

P.O. Box 1450

Alexandria, VA 22313-1450

or faxed to:

(703) 872-9306

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington. VA., Sixth Floor (Receptionist).

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Technology Center 2600 Customer Service Office whose telephone number is (703) 306-0377.

Young T. Tse
Primary Examiner
3/31/04